

PIC18F4685 - one of the Future Microcontrollers for memory intensive Applications

A special variant of MIOS is available for the PIC18F4685. The usage of this processor is (currently) only required for the next major step of MIDibox SID (V2), most other projects are running fine on a PIC18F452 (*MIDibox SEQ V3 will run on a [PIC18F4620](#)*)

Biggest advantages of this microcontroller: 96k internal flash (3 times more), 3328 bytes RAM (ca. 2 times more), 1024 bytes internal EEPROM (4 times more), and hardware compatibility to the PIC18F452 - therefore the same MBHP_CORE module can be used.

In difference to PIC18F452 or [PIC18F4620](#), the PIC18F4685 provides a CAN interface which allows to build up a network between multiple microcontrollers. The [MBNet protocol](#) has been defined to allow MIDiboxes to talk together

PIC18F4685 and PIC18F4682 are not 100% binary compatible to PIC18F452. RAM from 0x60-0x7f is not directly accessible. BANKED accesses have to be used instead.

Also See

- [Using the PIC18F4685](#)
- [Using the PIC18F4620 or PIC18F4520](#)

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