



M16 Interface

Add 16 MIDI I/O to your Core, SPI Slave Interface with up to 16 UARTs(MIDI I/O), based on low-cost FPGA...

ToDo

Some connection examples\\

Spi slave, share protocol and added commands

Features

- The FPGA internal clock works @88.67MHz.
- Fast 4 wires SPI in slave mode to control the board, 10Mb/s.
- Uses the default MIOS32_SPI_MIDI protocol, MIOS32 is ready-to-use with it.
- 16 UARTs on board, it's 16 MIDI ports.
- Each MIDI output has its own FIFO buffer of 1024 bytes, to queue the incoming MIDI from the SPI.
- Each MIDI output has its independent "Running Status", with Disable/Enable Command from SPI.
- There's a 64 word(32bits) FIFO for out-coming messages from the board.

- 3 independents groups of 16 GPIOs, configurable and settable by SPI Command.
- Can be stacked under a [dipBoard32 mbhp](#)

In MIOS32

datasheet

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